REMARKS

Applicant notes with appreciation the indication by the Examiner of allowable subject matter recited in Claims 2, 3, 4, and 9-23. Applicant further notes with appreciation the telephonic interview provided by the Examiner on February 10, 2004, to discuss U.S. Patent No. 5,218,246 of Lee, *et al.* and the amendments to Claims 1-6.

This Response amends Claims 1-6 to define the recited logic circuit in Claims 1-6 as a digital logic circuit. This Response further adds new Claims 24-27. New Claim 24 corresponds to original Claim 2 rewritten in independent form, which the Examiner indicates is allowable claim because the prior art does not disclose a plurality of XOR logic circuits coupled in parallel. New Claims 25-27 correspond to original Claims 3-5. These amendments present no new matter, and they present no new issues. Thus, consideration of the proposed amendments requires no further search. Claims 1-23, of which Claims 1, 6, 9, and 18 are independent are now pending in the application.

Rejection under 35 U.S.C. § 102

The Office Action rejects Claims 1 and 5-8 as being anticipated by U. S. Patent No. 5,218,246 of Lee, et al. (hereinafter "Lee"). Applicant respectfully traverses this rejection on the basis of the following arguments, and further contends that Lee fails to disclose all elements of these claims, as described below, and hence, does not anticipate the claimed invention.

For purposes of clarity in the discussion below, the respective claim rejections under 35 U.S.C. § 102 are discussed separately.

A. Rejection of Claims 1 and 5 under 35 U.S.C. § 102(b):

The Office Action rejects Claims 1 and 5 as being anticipated by Lee. Applicant respectfully traverses this rejection on the basis of the following arguments and the above amendments, and further contends that Lee fails to disclose all elements of these claims, as described below and hence, does not anticipate the claimed invention.

Lee discloses an analog XOR amplifier coupled to the bit lines of a static RAM. The analog XOR amplifier performs a comparison of the analog values read from the

static RAM and the results of the comparison are combined in an analog NOR circuit. The result thereof is finally amplified and converted into a CMOS signal by a sense amplifier.

Applicant's invention recited in amended Claims 1 and 5 are directed to *digital* logic circuits to perform an XOR logic function without the *digital* logic circuit entering an unstable state. Each *digital* logic circuit includes an input circuit and an output circuit. The input circuit converts a number of static input signals to a number complimentary dual rail domino output signals having one or more valid states. The output circuit performs a number of the XOR logic functions on the complimentary dual rail domino output signals without the *digital* logic circuit entering an unstable state. Consequently, the *digital* logic circuits of amended Claims 1 and 5 are well suited for use to generate a "finish" signal, which, in turn, can be used to start evaluation of the next stage in a data pipeline without the need for additional circuitry to gate or delay the finish signal to prevent a false start.

The inventions recited in amended Claims 1 and 5 distinguish patentability over the Lee patent. The Lee patent does not disclose a *digital* XOR logic circuit to perform an XOR logic function. It is well recognized that the XOR function is an important conceptual building block in digital logic systems. Therefore the *digital* logic circuits recited in amended Claims 1 and 5 are digital logic circuits to perform an XOR logic function without the *digital* logic circuit entering an unstable state. Furthermore, the Lee patent fails to disclose that the *digital* logic circuit includes an input circuit to convert a plurality of static input signals to a plurality of complimentary dual rail *domino* output signals having one or more valid states. That is, Lee reads data from a RAM in an analog format (i.e., millivolts) and manipulates the data in the analog format to avoid the use of *digital* comparators operated by turning MOS devices on and off at a very high speed. *See*, column 2, lines 29-37 of Lee.

The object of the circuits disclosed by Lee is to avoid performing a logic function on *digital* signals because of the switching noise associated with switching the devices on and off at a very high rate of speed and in addition to avoid the power bouncing problems associated with such switching speed. As such, Lee performs a logic function on a differential signal from a static RAM that is represented by two analog signals having

several hundred millivolts difference between them, received from the bit lines of the static RAM. *See*, column 4, line 65 to column 5, line 1 of Lee.

Accordingly, the Lee patent does not anticipate amended Claims 1 and 5, as such, Applicant requests the Examiner to reconsider and withdraw the rejection of Claims 1 and 5 under 35 U.S.C § 102(b).

B. Rejection of Claims 6-8 under 35 U.S.C. § 102(b):

The Office Action rejects Claims 6-8 as being anticipated by Lee. Applicant respectfully traverses this rejection on the basis of the following arguments and the above amendments, and further contends that Lee fails to disclose all elements of these claims, as described below and hence, does not anticipate the claimed invention.

The inventions recited in Claims 6-8, as amended, distinguish patentability over the Lee patent. The Lee patent is concerned with an analog XOR amplifier for comparing analog signals read from a static RAM having several hundred millivolts difference between them. Lee does not disclose a method for performing a near simultaneous comparison of multiple bits in a *digital* logic circuit using a logical XOR function in a manner that avoids the XOR function hazard of the logical XOR function as recited by amended Claims 6. Furthermore, the Lee patent fails to disclose that the method includes a step of generating a plurality of dual rail *domino* output signals from a plurality of input signals in a manner that avoids an unstable state in a *digital* logical XOR circuit to avoid the XOR function hazard in the *digital* logical XOR circuit.

In contrast, Claims 6-8, as amended, each recite a method for performing a near simultaneous comparison of multiple bits in a *digital* logic circuit using a logical XOR function in a manner that avoids an XOR function hazard of the logical XOR function. The method of amended Claim 6, and thus Claims 7-8, avoids what is known in the art as a "function hazard" in part by generating a number of dual rail *domino* signals from a number of input signals in a manner that avoids an unstable state in a *digital* logical XOR circuit to avoid the XOR function hazard in the *digital* logical XOR circuit. Nowhere does Lee disclose such a feature. Lee is concerned with avoiding the use of signals in a

digital format and as such performs a comparison of bit line values read from a static RAM using differential signals in an analog format. Nowhere does Lee disclose a method for performing a near simultaneous comparison of multiple bits in a *digital* logic circuit using a logical XOR function in a manner that avoids an XOR function hazard of the logical XOR function.

Accordingly, Claims 6-8, as amended, are not anticipated by the Lee patent. Applicant requests the Examiner to reconsider and withdraw the rejection of Claims 6-8 under 35 U.S.C. § 102(b).

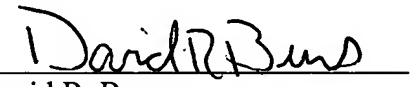
New Claims 24-27

New Claims 24-27 are not anticipated by nor are they rendered obvious by the cited references either alone or in combination. Specifically, new Claim 24 corresponds to original Claim 2 rewritten in independent form to include all the limitations of Claim 1. New Claims 25-27 in like manner correspond to original Claims 3-5. The Examiner indicates that original Claim 2 would be allowable if rewritten in independent form including all of the limitations of independent Claim 1. Accordingly, Applicant contends that new Claims 24-27 are allowable for at least this reason.

CONCLUSION

For the foregoing reasons, Applicants contend that Claims 1-27 are patentable and in condition for allowance. If there are any remaining issues, an opportunity for an interview is requested prior to the issuance of another Office Action. If the above arguments are not deemed to place this case in condition for allowance, the Examiner is urged to call Applicants' representative at the telephone number listed below.

Respectfully submitted,
LAHIVE & COCKFIELD, LLP



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